**CLAIMS**

1. A memory cell, comprising:

a capacitor having a dielectric layer interposing first and second vertically disposed electrodes;

an insulating lining located over the capacitor;

a transistor gate extension passing over the capacitor; and

a spacer isolating an end of one of the capacitor electrodes from the transistor gate extension, the spacer having a first non-planar profile configured to engage a second non-planar profile comprising ends of the one of the capacitor electrodes and the insulating lining.

2. The memory cell of claim 1 wherein the second non-planar profile is a mirror image of the first non-planar profile.

3. The memory cell of claim 1 further comprising an anti-reflection coating (ARC) layer between at least portions of the one of the capacitor electrodes and the transistor gate extension.

4. The memory cell of claim 3 wherein the spacer includes:

a body having a body width; and

a protrusion extending from the body a distance substantially equal to the body width;

wherein the second non-planar profile includes a recess formed by an offset between the ends of the one of the capacitor electrodes and the insulating lining.

5. The memory cell of claim 1 wherein the spacer includes a nitride layer and an oxide layer located over the nitride layer.

6. The memory cell of claim 1 wherein the spacer includes a silicon nitride layer and an oxide layer located over the silicon nitride layer.

7. A memory array, comprising:

a plurality of capacitive elements each including:

a dielectric layer interposing first and second vertically disposed electrodes;

an insulating lining located over one of the first and second electrodes; and

a spacer having a first non-planar profile configured to engage a second non-planar profile comprising ends of the one of the first and second electrodes and the insulating lining; and

a passing gate extending over at least one of the plurality of capacitive elements and coupling ones of a plurality of transistors each adjacent ones of the plurality of capacitive elements.

8. A method of manufacturing a memory cell, comprising:

forming a capacitor having two electrodes in an opening in a substrate, wherein termini of one of the electrodes extend over and substantially parallel to the substrate;

forming a lining over and conforming to a profile of the capacitor, the lining having termini interiorly offset from the termini of the one of the capacitor electrodes;

forming a gate electrode extension passing over the capacitor; and

forming a spacer isolating a terminus of the one of the capacitor electrodes from the gate electrode extension, the spacer including a protrusion conforming to a recess defined by one of the lining termini and the terminus of the one of the capacitor electrodes.

9. The method of claim 8 wherein forming the lining includes depositing an electrically insulating material and isotropically etching the electrically insulating material.

10. The method of claim 8 further comprising forming an anti-reflection coating (ARC) layer over and conforming to the lining, the ARC layer having termini exteriorly offset from the lining termini.

11. The method of claim 10 wherein the lining comprises a material to which an isotropic etching process is selective, wherein the lining termini are defined by the etching process after forming the ARC layer, whereby the lining termini undercut the ARC layer termini.

12. The method of claim 10 wherein the each of the recesses defined by one of the lining termini and one of the capacitor termini is further defined by one of the ARC layer termini.

13. The method of claim 8 wherein the capacitor includes:

a first electrode having termini protruding from the opening;

a second electrode substantially conforming to the first electrode and the substrate; and

a dielectric layer isolating the second electrode from the first electrode; wherein

the lining termini are interiorly offset from termini of the second electrode.

14. The method of claim 8 wherein forming the spacers includes forming a first spacer layer and forming a second spacer layer over the first spacer layer, wherein the protrusions are integral to the first spacer layer.

15. The method of claim 14 wherein the first spacer layer comprises nitride and the second spacer layer comprises oxide.

16. The method of clam 14 wherein the first spacer layer comprises a material selected from the group consisting of:

$Si_3N_4$;

CN;

SiOC;

SiC;

SiCN; and

SiO2.

17. The method of claim 14 wherein at least one of the first and second spacer layers is formed by a process selected from the group consisting of:

gaseous diffusion;

CVD;

PECVD;

PVD; and

ALD.

18. The method of claim 14 wherein the first spacer layer has a thickness ranging between about 100 Angstroms and about 500 Angstroms.

19. The method of claim 14 wherein the second spacer layer has a thickness ranging between about 200 Angstroms and about 700 Angstroms.

20. The method of claim 8 wherein the lining comprises $Si_3N_4$.

21. The method of claim 8 wherein the gate electrode extension has a width that is less than about 130 nm.